Investigation of performance and characteristics of junctionless carbon nanotube field effect transistors with non-equilibrium greens function method

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In this work by employing numerical two- and three-dimensional simulations we study the electrical performance characteristics and short channel behavior of various multi-gate transistors based on advanced SOI technology. These include single-gate, double-gate, triple-gate and gate-all-around nanowire FETs with different channel material, namely Carbon Nanotube (CNT), Silicon Nanowire (NW) and III-V compound semiconductors, all most promising candidates for future of nanoscale CMOS technologies. Also, a new type of transistor called Junctionless Nanowire Transistor (JLT) is presented and several simulations are carried out to study its electrical characteristics. We study the influence of device properties such as different channel material, dimensions, and doping concentration as well as quantum effects on the performance of multi-gate SOI transistors. For the modeled n-channel nanowire devices we found that at very small cross-sections the nanowires with silicon channel are more immune to short channel effects. Interestingly, the mobility of the channel material is not as significant in determining the device performance in ultra-scale channels as other material properties such as the dielectric constant and the effective mass. Better electrostatic control is achieved in materials with smaller dielectric constant and smaller source-to-drain tunneling currents are observed in channels with higher transport effective mass. This explains our results on CNT/Nanowire-based devices. In addition to utilizing the commercial TCAD software (Silvaco TCAD), we have developed a two-dimensional Schrödinger-Poisson solver based on the non-equilibrium Green’s functions (NEGF) formalism in the framework of effective mass approximation with the open NEGF simulation package MOSCNT. This
allows exploring the influence of quantum effects on electrical performance of ultra-scaled device with heavily n-type-doped CNT-channel along with junctionless structure, namely as Junctionless Tunneling Carbon Nanotube Filed Effect Transistor (JL-TCNTFET). We have implemented conventional mode-space methodologies in our 2D quantum-mechanical simulator and moreover introduced new codes to deal with electrical characteristics in the aforementioned device structure which has excellent reliability and validity with junctionless structure. In chapter 1, the conventional size scaling of Silicon CMOS has been reviewed and the benefits of Moore’s law, in terms of speed and power, have been discussed. The challenges of scaling beyond 22 nm technology nodes have been classified into five groups, which are gate control, current output, capacitance, power/performance ratio, and variation/reliability. Solutions for beyond 22 nm devices, named as technology boosters, have been discussed and extended into the proposed junctionless structure with novel Si channel material. In chapter 2, the simulations are carried out using the Matrix Laboratory (MATLAB) tool in addition to the Silvaco Atlas Technology Computer-Aided Design (TCAD) software, in order to investigate different structure of multi-gate JLT in terms of gate control, energy band diagram and transfer characteristics. In the first place, the unique conduction mechanism and electrical characteristics for JLT for Si channel material have been discussed. In the second place, due to the fact that JLT does not require any metallurgical junction in the source-channel and drain-channel interface and it has better electrical characteristics and less variability rather than traditional MOSFET, we have simulated the Junctionless Tunnel Filed Effect Transistor (JL-TFET) which gives the advantage of JL-FET and Tunnel FET (TFET) combined together. In chapter 3, a Gate-all-around Junctionless Carbon-based Tunnel FET (JL-TCNTFET) is proposed and investigated using 2-D Non-Equilibrium Green’s Function approach with mode-space algorithm (MS). The JL-TCNFET is a CNT-channel heavily degenerately doped Junctionless Field Effect Transistor (JL-FET) which uses one fixed P-type Gate (P-Gate) in spite of utilizing main Control Gate (C-Gate) with different workfunctions. In this structure, the privileges of Junctionless FET (JL-FET) and Tunneling FET (TFET) are blend together. Afterwards, according to performance enhancement of JL-TCNTFET with the principles of gate workfunctions engineering method, we have utilized the linear descending workfunction of gate, the linear ascending workfunction of gate and the triple metal gate features for proposing of three novel structures of the JL-TCNTFET, namely as Junctionless Linear Descending workfunction TFET (JL-LDWTFET), Junctionless Linear Ascending workfunction TFET (JL-LAWTFET) and Junctionless Triple Metal Gate TFET (JL-TMTFET), respectively. Simulations have shown that JL-TMTFET compared with another proposed structure has demonstrated a larger ON current (ION), a larger ON/OFF current ratio (ION/IOFF),
a superior ambipolar characteristic, a shorter delay time. In chapter 4, we have investigated the 40 nm n-type Gate-all-around Junctionless Tunnel FET (JL-TNWFET) and the impact of variation of various amount of uniaxial tensile strain on the performance parameters of the JL-TNWFET is discussed. We achieved superior results of different performance parameters by taking into account the highly uniaxial strain (1GPa)

Keywords : Nano transistor

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