Design and Simulation of a High Speed and Low Power 32-Bit Multiplier Based on Booth Algorithm and Wallace Tree Hybrid Structure in 0.18µm CMOS Technology

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Abstract: Parallel multiplier is an important part of the microprocessor and the DSP processors;The performance of this block has a great impact on the overall chip performance. The recent advancements in different scientific and technology fields demand heavy and time consuming simulation setups, which further emphasizes the significance of the multiplication process in modern digital processing systems which are the backbone of the most of the today computer systems. The reduction of power consumption is an important design parameter along with delay reduction in modern digital system design. Since the increment of the operation speed and the decrement of the power consumption have strong design contradiction to each other, therefore, in most of the recent works only improvement of one of these two parameters has been targeted. In this thesis and for the design and simulation of the multiplier and its sub-blocks, the standard 0.18µmCMOS process with 1.8V supply voltage has been employed. All sub-blocks of the multiplier have been designed in transistor level. By means of analytical expressions and simulation results, the advantages of the proposed system concerning the reduced power consumption, reduced active area and power consumption which translates into the improved speed of operation are demonstrated in different sections of the thesis. In this thesis and for the design and simulation of the multiplier and its sub-blocks, the standard 0.18µmCMOS process with 1.8V supply voltage has been employed. All sub-blocks of the multiplier have been designed in transistor level and by means of analytical expressions and simulation results, the advantages of the proposed system concerning the reduced power consumption, reduced active area and power consumption which translates

into the improved speed of operation are demonstrated in different sections of the thesis. The simulation results demonstrate the correct functionality of the proposed architecture and confirm the theoretical assumptions which have been made during the system and circuit level implementations. Based on the obtained results, the multiplier operates successfully at the clock frequency of 2GHz while the delay of the proposed 32 bit multiplier is equal to 4.39ns. The number of the transistors used in the multiplier circuit and the active area occupied on the chip by the proposed multiplier are 29859 and 0.825mm2, respectively. The delay and transistor count for proposed Booth encoding circuit are 176ps and 46, respectively; the circuit of the proposed 4-2 compressor has 58 transistors andits delay value is equal to 260ps.

Keywords : Parallel Booth Multiplier, Booth Encoder-Decoder, 4-2 Compressor, High Speed